

**WHAT IS CLAIMED IS:**

1 *Sub*  
2 *A10* 1. A data processing apparatus comprising:  
3 a register file comprising a plurality of registers, each of  
4 said plurality of registers having a corresponding register  
5 number;  
6 a first functional unit group connected to said register file  
7 and including a plurality of first functional units, said first  
8 functional unit group responsive to an instruction to  
9 receive data from one of said plurality of registers  
10 corresponding to an instruction-specified first operand  
11 register number at a first operand input,  
12 operate on said received data employing an instruction-  
13 specified one of said first functional units, and  
14 output data to one of said plurality of registers  
15 corresponding to an instruction-specified first destination  
16 register number from a first output;  
17 a second functional unit group connected to said register  
18 file and including a plurality of second functional units, said  
19 second functional unit group responsive to an instruction to  
20 receive data from one of said plurality of registers  
21 corresponding to an instruction-specified second operand  
22 register number at a second operand input,  
23 operate on said received data employing an instruction-  
24 specified one of said second functional units, and  
25 output data to one of said plurality of registers  
26 corresponding to an instruction-specified second destination  
27 register number from a second output;  
28 a first comparator receiving an indication of said first  
29 operand register number of a current instruction and an  
indication of said second destination register number of an

30 immediately preceding instruction, said first comparator  
31 indicating whether said first operand register number of said  
32 current instruction matches said second destination register  
33 number of said immediately preceding instruction; and

34 a first register file bypass multiplexer connected to said  
35 register file, said first functional unit group, said second  
36 functional unit group and said first comparator having a first  
37 input receiving data from said register corresponding to said  
38 first operand register number of said current instruction, a  
39 second input connected to said second output of said second  
40 functional unit group and an output supplying an operand to said  
41 first operand input of said first functional unit group, said  
42 first multiplexer selecting said data from said register  
43 corresponding to said first operand number of said current  
44 instruction if said first comparator fails to indicate a match  
45 and selecting said second output of said second functional unit  
46 group if said first comparator indicates a match.

1 2. The data processing apparatus of claim 1, wherein said  
2 register file, said first functional unit group, said second  
3 functional unit group, said first comparator and said first  
4 register file bypass multiplexer operate according to an  
5 instruction pipeline comprising:

6 a first pipeline stage consisting of a register read  
7 operation from said register file and a first half of operation  
8 of a selected functional unit of said first and said second  
9 functional unit groups, and

10 a second pipeline stage consisting of a second half of  
11 operation of said selected functional unit of said first and said  
12 second functional unit groups and a register write operation to  
13 said register file,

14 wherein the sum of the time of said register read operation  
15 and said register write operation equals approximately the sum of

16 the time of said first and second halves of operation of a  
17 slowest of said functional units of said first and second  
18 functional unit groups

1 3. The data processing apparatus of claim 1, further  
2 comprising an output register having an input connected to said  
3 second output of said second functional unit group and an output  
4 connected to said register file for temporarily storing said  
5 output of said second functional unit group prior to storing in  
6 said register corresponding to said second destination register  
7 number,

8 wherein said first comparator further receives an indication  
9 of said second destination register number of a second preceding  
10 instruction, said first comparator further indicating whether  
11 said first operand register number of said current instruction  
12 matches said second destination register number of said second  
13 preceding instruction, and

14 wherein said multiplexer further has a third input connected  
15 to said output register output, said multiplexer selecting said  
16 output register output if said first comparator indicates a  
17 match.

1 4. The data processing apparatus of claim 3, wherein said  
2 register file, said first functional unit group, said second  
3 functional unit group, said first comparator, said first register  
4 file bypass multiplexer, and said output register operate  
5 according to an instruction pipeline comprising:

6 a first pipeline stage consisting of a register read  
7 operation from said register file;

8 a second pipeline stage consisting of an operation of a  
9 selected functional unit of said first and second functional unit  
10 groups; and

11 a third pipeline stage consisting of a register write  
12 operation to said register file,  
13 wherein the time of said register read operation and the  
14 time of said register write operation are each equal  
15 approximately to the time of operation of a slowest of said  
16 selected functional units of said first and second functional  
17 unit groups.

AI 1 5. The data processing apparatus of claim 1, said first  
2 comparator further receiving an indication of said first  
3 destination register of said immediately preceding instruction,  
4 said first comparator further indicating whether said first  
5 operand register number of said current instruction matches said  
6 first destination register number of said immediately preceding  
7 instruction, said first multiplexer further having a third input  
8 connected to said first output of said first functional unit  
9 group, and said first multiplexer selecting said first output of  
10 said first functional unit group if said first comparator  
11 indicates a match.

1 6. The data processing apparatus of claim 1, said first  
2 functional unit group further responsive to an instruction to  
3 receive data from one of said plurality of registers  
4 corresponding to an instruction-specified third operand register  
5 number at a third operand input,

6 said apparatus further comprising:

7 a second comparator receiving an indication of said  
8 third operand register number of a current instruction and an  
9 indication of said second destination register number of said  
10 immediately preceding instruction, said second comparator  
11 indicating whether said third operand register number of said  
12 current instruction matches said second destination register  
13 number of said immediately preceding instruction; and

14 a second register file bypass multiplexer connected to  
15 said register file, said first functional unit group, said second  
16 functional unit group and said second comparator having a first  
17 input receiving data from said register corresponding to said  
18 third operand register number of said current instruction, a  
19 second input connected to said second output of said second  
20 functional unit group and an output supplying an operand to said  
21 third operand input of said first functional unit group, said  
22 second multiplexer selecting said data from said register  
23 corresponding to said third operand number of said current  
24 instruction if said second comparator fails to indicate a match  
25 and selecting said second output of said second functional unit  
26 group if said second comparator indicates a match.

1 7. The data processing apparatus of claim 6, said first  
2 comparator further receiving an indication of said first  
3 destination register of said immediately preceding instruction,  
4 said first comparator further indicating whether said first  
5 operand register number of said current instruction matches said  
6 first destination register number of said immediately preceding  
7 instruction, said first multiplexer further having a third input  
8 connected to said first output of said first functional unit  
9 group, said first multiplexer selecting said first output of said  
10 first functional unit group if said first comparator indicates a  
11 match,

12 said second comparator further receiving an indication of  
13 said first destination register of said immediately preceding  
14 instruction, said second comparator further indicating whether  
15 said third operand register number of said current instruction  
16 matches said first destination register number of said  
17 immediately preceding instruction, said second multiplexer  
18 further having a third input connected to said first output of  
19 said first functional unit group, and said second multiplexer

20 selecting said first output of said first functional unit group  
21 if said second comparator indicates a match.

1 8. The data processing apparatus of claim 1 further  
2 comprising:

3 a third comparator receiving an indication of said second  
4 operand register number of a current instruction and an  
5 indication of said second destination register number of an  
6 immediately preceding instruction, said third comparator  
7 indicating whether said second operand register number of said  
8 current instruction matches said second destination register  
9 number of said immediately preceding instruction; and

10 a third register file bypass multiplexer connected to said  
11 register file, said first functional unit group, said second  
12 functional unit group and said third comparator having a first  
13 input receiving data from said register corresponding to said  
14 second operand register number of said current instruction, a  
15 second input connected to said second output of said second  
16 functional unit group and an output supplying an operand to said  
17 second operand input of said second functional unit group, said  
18 third multiplexer selecting said data from said register  
19 corresponding to said second operand number of said current  
20 instruction if said third comparator fails to indicate a match  
21 and selecting said second output of said second functional unit  
22 group if said third comparator indicates a match.

1 9. The data processing apparatus of claim 8, said third  
2 comparator further receiving an indication of said first  
3 destination register number of an immediately preceding  
4 instruction, said third comparator indicating whether said second  
5 operand register number of said current instruction matches said  
6 first destination register number of said immediately preceding  
7 instruction, said third multiplexer further having a third input

8 connected to said first output of said first functional unit  
9 group, and said third multiplexer further selecting said first  
10 output of said first functional unit group if said third  
11 comparator indicates a match.

1 10. The data processing apparatus of claim 1 further  
2 comprising a third functional unit group connected to said  
3 register file, wherein said third functional unit group's  
4 register file output data is available for register file bypass  
5 solely within the third functional unit group itself.

1 11. A data processing apparatus comprising:

2 a first register file comprising a plurality of registers,  
3 each of said plurality of registers having a corresponding  
4 register number;

5 a second register file comprising a plurality of registers,  
6 each of said plurality of registers having a corresponding  
7 register number;

8 a first functional unit group including an input connected to  
9 said first and second register files, an output connected to said  
10 first register file, and a plurality of first functional units,  
11 said first functional unit group responsive to an instruction to

12 receive data from one of said plurality of registers in  
13 said first and second register files corresponding to an  
14 instruction-specified first operand register number at a  
15 first operand input,

16 operate on said received data employing an instruction-  
17 specified one of said first functional units, and

18 output data to one of said plurality of registers in  
19 said first register file corresponding to an instruction-  
20 specified first destination register number from a first  
21 output;

22 a second functional unit group including an input connected  
23 to said first and second register files, an output connected to  
24 said second register file, and a plurality of second functional  
25 units, said second functional unit group responsive to an  
26 instruction to

27 receive data from one of said plurality of registers in  
28 said first and second register files corresponding to an  
29 instruction-specified second operand register number at a  
30 second operand input,

31 operate on said received data employing an instruction-  
32 specified one of said second functional units, and

33 output data to one of said plurality of registers in  
34 said second register file corresponding to an instruction-  
35 specified second destination register number from a second  
36 output; and

37 a first crosspath connecting said second register file to  
38 said first functional unit group comprising

39 a first crosspath comparator, wherein, if said first  
40 operand register is in said second register file, said  
41 comparator receives an indication of said first operand  
42 register number of a current instruction and an indication  
43 of said second destination register number of a preceding  
44 instruction, and said first crosspath comparator indicates  
45 whether said first operand register number of said current  
46 instruction matches said second destination register number  
47 of said preceding instruction, and

48 a first crosspath multiplexer connected to said second  
49 register file, said first functional unit group, said second  
50 functional unit group and said first crosspath comparator  
51 having a first input receiving data from said register  
52 corresponding to said first operand register number of said  
53 current instruction, a second input connected to said second  
54 output of said second functional unit group and an output



55 supplying an operand to said first operand input of said  
56 first functional unit group, wherein, if said first operand  
57 register is in said second register file, said first  
58 crosspath multiplexer selects said data from said register  
59 corresponding to said first operand number of said current  
60 instruction if said first crosspath comparator fails to  
61 indicate a match and selects said second output of said  
62 second functional unit group if said first crosspath  
63 comparator indicates a match.

1 12. The data processing apparatus of claim 11 further  
2 comprising a second crosspath connecting said first register file  
3 to said second functional unit group.

1 13. The data processing apparatus of claim 11, said first  
2 crosspath further comprising a first crosspath register latching  
3 said crosspath multiplexer's output for said first functional  
4 unit group's first operand input.

1 14. The data processing apparatus of claim 11 further  
2 comprising a third functional unit group including an input  
3 connected to said first and second register files, an output  
4 connected to said first register file, and a plurality of third  
5 functional units, said third functional unit group responsive to  
6 an instruction to

7 receive data from one of said plurality of registers in said  
8 first and second register files corresponding to said  
9 instruction-specified first operand register number at a third  
10 operand input,

11 operate on said received data employing an instruction-  
12 specified one of said third functional units, and

13 output data to one of said plurality of registers in said  
14 first register file corresponding to an instruction-specified  
15 third destination register number from a third output,

16 said first crosspath further connecting said second register  
17 file to said third functional unit group, and said first  
18 crosspath multiplexer further having an output supplying an  
19 operand to said third operand input of said third functional unit  
20 group.

1 15. The data processing apparatus of claim 11 further  
2 comprising:

3 a first input comparator receiving an indication of said  
4 first operand register number of a current instruction, said  
5 first comparator indicating whether said first operand register  
6 number is in said first register file or said second register  
7 file; and

8 a first input multiplexer having a first input connected to  
9 said first register file, a second input connected to said first  
10 crosspath, and an output connected to said first functional unit  
11 group, said first input multiplexer selecting said first input if  
12 said first input comparator indicates said register corresponding  
13 to said first operand number is in said first register file, and  
14 selecting said second input if said first input comparator  
15 indicates said register corresponding to said first operand  
16 number is in said second register file.

1 16. The data processing apparatus of claim 15 further  
2 comprising a fourth functional unit group including an input  
3 connected to said first and second register files, an output  
4 connected to said first register file, and a plurality of fourth  
5 functional units, said fourth functional unit group responsive to  
6 an instruction to

7 receive data from one of said plurality of registers in said  
8 first or second register files corresponding to an instruction-  
9 specified fourth operand register number at a fourth operand  
10 input,

11 operate on said received data employing an instruction-  
12 specified one of said fourth functional units, and

13 output data to one of said plurality of registers in said  
14 first register file corresponding to an instruction-specified  
15 fourth destination register number from a fourth output,

16 said first input comparator further receiving an indication  
17 of said fourth destination register number of an immediately  
18 preceding instruction, said input first comparator indicating  
19 whether said first operand register number of said current  
20 instruction matches said fourth destination register number of  
21 said immediately preceding instruction, and

22 said first input multiplexer further having a third input  
23 connected to said fourth output of fourth functional unit group,  
24 said first multiplexer selecting said fourth output of said  
25 fourth functional unit group if said first input comparator  
26 indicates a match.

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